REMARKS

Objections

The Examiner has objected to the specification because of informalities in paragraphs [0053], [0060] and [0062]. Applicant has amended these paragraphs to overcome the Examiner's objections.

Claims 20-21 have been objected to for various informalities. Applicant has amended Claims 19 and 20, thereby overcoming the Examiner's objections to Claims 20-21.

Rejections under 112, second paragraph

Claims 1-21 and 25-30 have been rejected under 35 U.S.C. 112, second paragraph as being indefinite. The Examiner objects to the use of the term 'floating gate'. Applicant has amended Claims 1, 6, 10 and 14 to replace the 'third floating gate" and the 'third control gate" with 'a first gate and 'a second gate located over the first gate', thereby clarifying Claims 1-14.

Applicant has amended Claims 15 and 17 to replace the 'second floating gate' and the 'second control gate' with 'a first gate' and a second gate located over the first gate', thereby clarifying Claims 15-21.

Applicant has amended Claim 25 to replace 'a control gate of the third transistor' and 'a floating gate of the third transistor' with 'a first gate' and 'a second gate', thereby clarifying Claims 25 and 26.

Applicant has amended Claim 27 to recite 'a second transistor having … a first gate, and a second gate located over the first gate', thereby clarifying Claims 27-30.

Claims 1-5 and 10-14 have been rejected under 35 U.S.C. 112, second paragraph as being incomplete for omitting essential structural cooperative relationships. The

Examiner questions how the third transistor actually relates to the first and second transistors. The Applicant has amended Claim 1 to recite "an input terminal, wherein a drain of the first transistor, a drain of the third transistor and the second gate of the third transistor are each coupled to the input terminal". Similarly, Claim 10 has been amended to recite "electrically connecting a drain of the first transistor, a drain of the third transistor and the second gate". Consequently, Claims 1-5 and 10-14 meet the requirements of 35 U.S.C. 112, second paragraph.

Claim 7 has been amended to eliminate 'the reference voltage circuit'. As a result, Claim 7 does not exhibit any antecedent basis problems.

Rejections under 103(a)

Claims 1-2, 4-5, 10-11 and 13-14 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Pathak (U.S. Patent No. 6,411,549) in view of Madurawe (U.S. Patent No. 6,532,170).

As described above, Claim 1 has been amended to recite 'an input terminal, wherein a drain of the first transistor, a drain of the third transistor and the second gate of the third transistor are each coupled to the input terminal'.

The Examiner indicates that memory cell C00, memory cell C01 and reference transistor 51 of Pathak correspond with the first, second and third transistors, respectively, as recited by Claim 1. However, Pathak fails to teach that the drain of memory cell C00 (or C01) is coupled to the same terminal as the drain of reference transistor 51 and the gate of reference transistor 51. For this reason, Pathak fails to teach 'a drain of the first transistor, a drain of the third transistor and the second gate of the third transistor are each coupled to the input terminal' as

recited by amended Claim 1. Madurawe fails to remedy this deficiency of Pathak.

In addition, Pathak clearly teaches that the floating gates of memory cells C00-C01 are not electrically coupled. The Examiner argues that Madurawe remedies this deficiency of Pathak. Madurawe teaches a memory cell 400 that includes two transistors (i.e., a read transistor 710 and a program transistor 715), which share a common floating gate 735. The Examiner suggests that it would be obvious for memory cells C00 and C01 of Pathak to share a common floating gate. However, Pathak teaches that memory cells C00 and C01 are separate memory cells, each capable of independently storing a data value. If these memory cells C00 and C01 were modified to share the same floating gate as suggested by the Examiner, then these memory cells C00 and C01 would necessarily have to store the same data value, thereby unduly limiting the functionality of the associated memory array 13. For this reason, it is not obvious to combine Pathak and Madurawe.

For these reasons, Claim 1 is allowable over Pathak in view of Madurawe. Claims 2 and 4-5, which depend from Claim 1, are allowable over Pathak in view of Madurawe for at least the same reasons as Claim 1.

Claim 10, which has been amended to recite 'electrically connecting a drain of the first transistor, a drain of the third transistor and the second gate' is allowable over Pathak and Madurawe for reasons similar to Claim 1. Claims 11 and 13-14, which depend from Claim 10, are allowable over Pathak in view of Madurawe for at least the same reasons as Claim 10.

Applicant notes the allowance of Claims 22-24.

The Examiner has indicated that Claims 15, 25 and 27 would be allowable if rewritten or amended to overcome the rejections under 35 U.S.C. 112, second paragraph. As described above, the Applicant has amended Claims 15, 25 and 27 to overcome the rejections under 35 U.S.C. 112, thereby placing Claims 15, 25 and 27 in condition for allowance.

Claims 3, 6-9, 12, 16-21, 26 and 28-30 have been objected to as being dependent upon a rejected base claim. The Examiner has indicated that these claims would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicants believe that base claims 1, 10, 15, 25 and 27 are allowable in view of the arguments provided above. Consequently, Applicants are not amending Claims 3, 6-9, 12, 16-21, 26 and 28-30 at this time.

CONCLUSION

Claims 1-30 are pending in the present Application. Claims 22-24 are allowed, and Claims 3, 6-9, 12, 15-21, 25-30 are in condition for allowance. Reconsideration and allowance of Claims 1-2, 4-5, 10-11 and 13-14 is respectfully requested. If there are any questions, please telephone the undersigned at (925) 895-3545 to expedite prosecution of this case.

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